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Attorney's Docket No.: 10559 101002 / P7635C  
Intel CorporationREMARKS

Claims 2-15 are pending, with claims 2, 6, and 15 being independent. Claims 2, 6, 11, and 15 have been amended. No new matter has been added. Reconsideration and allowance of the above-referenced application are respectfully requested.

Rejections Under 35 U.S.C. §101

Claim 15 stands rejected under 35 U.S.C. §101 as allegedly being directed to non-statutory subject matter. The Applicant respectfully traverse this contention by the Office. The Federal Circuit has long held that the claimed invention as a whole must be useful and accomplish a practical application; i.e., it must produce a "useful, concrete and tangible result." (*State Street Bank & Trust Co. v. Signature Financial Group Inc.*, 149 F. 3d 1368, 47 USPQ2d 1596, 1601-02 (Fed. Cir. 1998).) Amended claim 15 recites, among other features: "to form a final two-dimensional scaled image of a lower definition ... and display the final two-dimensional scaled image" (emphases added). Claim 15, as a whole, is useful and accomplishes a practical application by producing and displaying a "two-dimensional scaled image of a lower definition" (tangible output) for each high definition television image that appears in a video sequence of images for display on a computer monitor.

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Therefore, withdrawal of the rejection of claim 1 under 35 U.S.C. § 101 is respectfully requested.

Rejections Under 35 U.S.C. § 112

Claims 2-5, 11-13 and 15 stand rejected under 35 U.S.C. §112, second paragraph, as being indefinite for lacking antecedent bases. Applicant has obviated these rejections by amending claims 2, 11, and 15. Therefore, withdrawal of the rejection of all claims under 35 U.S.C. § 112, second paragraph is respectfully requested.

Rejections Under 35 U.S.C. §103

Claims 2-15 stand rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over U.S. Patent No. 5,831,592 issued to Cahill, III (hereinafter "Cahill") in view of Applicant's admitted prior art (page 1 to page 3, line 7 of the present specification; hereinafter "AAPA"). This contention is respectfully traversed.

Initially, there is no motivation or suggestion to combine AAPA with Cahill. In fact, Cahill teaches away from this hypothetical Cahill-AAPA combination by disclosing that "when the bitmap is reduced for display, rows of the bitmap may be skipped." (Emphases added; Col. 21, lines 28-29 and Table V.) In contrast, skipping rows is not desired as stated on page 3, lines 1-7 of the present application. Thus, contrary to the

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Office's assertion, there is no motivation or suggestion to combine AAPA with Cahill.

Even if AAPA could be combined with Cahill, a *prima facie* case of obviousness has not been established because the hypothetical Cahill-AAPA combination does not teach or suggest all the elements of independent claims 2, 6, and 15. For example, contrary to the Office's contention, the portion of Cahill cited by the Office (Col. 11, line 27 to Col. 12 line 50) does not teach or suggest "reading locations from the memory at an image update rate to fetch first pixels in the image, which are vertically contiguous in the image" (emphases added) as recited in claim 2.

Contrary to the Office's contention, the cited portion of Cahill merely discloses using DDA-based processing in the capture controllers to "determine an integer difference value ..., [which] determines the filtering scheme implemented by the appropriate capture filter. For horizontal capture filters 702, 706, and 710, the integer difference value is the number of consecutive pixels in a row used during horizontal filtering. For vertical capture filter 718, the difference value is the number of consecutive pixels in vertical filtering" (emphases added; Col. 12, lines 15-26). Nowhere is there mention of an "image update rate", let alone "reading locations from the memory at an image update rate to fetch first pixels in the

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image, which are vertically contiguous in the image" (emphases added) as recited in claim 2.

In addition, Cahill does not teach "reading the vertically scaled set of pixels from the memory at an image display rate and horizontally scaling the vertically scaled set of pixels at the image display rate" (emphases added) as recited in claim 2. In fact, Cahill teaches away from claim 2 by stating "display interface 508 receives, scales and transmits data corresponding to portions of the image to be displayed without creating a scaled bitmap containing the scaled data for the entire image." (Emphasis added; Col. 15, lines 28-32; and Abstract lines 1-5.) Furthermore, the cited portions of Cahill (Figs. 11, 13, and 14) do not show a memory from which the stored "vertically scaled set of pixels" can be read at an "image display rate" as recited in claim 2. (See, e.g., Col. 20, line 54 to Col. 21, line 12 of Cahill, stating that the data is transmitted from the adder 1308 (Fig. 13) in vertical display scaler 1104 (Fig. 11) directly to the horizontal display scalers 1110, 1114 and 1118 (Fig. 14).)

Thus, Cahill does not disclose the features of independent claim 2, and AAPA is neither asserted to show such claimed features nor does so teach or suggest. Therefore, the hypothetical Cahill-AAPA combination does not teach or suggest each and every element of claim 2 and claim 2 should be in condition for allowance.

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Independent claims 6 and 15 recite similar features as claim 1 and are patentably distinguishable over the hypothetical Cahill-AAPA combination for analogous reasons to those discussed for independent claim 2. For example, claim 6 recites, among other features: "produce a vertically scaled image of contiguous, vertically scaled, horizontal pixels in the memory and to read pixels of the vertically scaled image only after the entire vertically scaled image has been formed, at an image display rate and horizontally scale pixels of the vertically scaled image at the image display rate ....".

Claim 15 recites, among other features: "read locations from the memory at an image update rate to fetch first pixels in the image, ...; and after said vertically scaling of the entire image, read the vertically scaled set of pixels from the memory at an image display rate and horizontally scaling the vertically scaled set of pixels at the image display rate ...." Thus, independent claims 6 and 15 should also be in condition for allowance.

Since claims 3-5 and 7-14 depend generally from independent claims 2 or 6, these dependent claims are patentably distinguishable over Cahill or AAPA, either alone or in combination for at least the reasons provided above for claim 2.

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Intel CorporationConcluding Comments

It is believed that all of the pending claims have been addressed in this paper. However, failure to address a specific rejection, issue or comment, does not signify agreement with or concession of that rejection, issue or comment. In addition, because the arguments made above are not intended to be exhaustive, there may be reasons for patentability of any or all pending claims (or other claims) that have not been expressed. Finally, nothing in this paper should be construed as an intent to concede any issue with regard to any claim, except as specifically stated in this paper, and the amendment of any claim does not necessarily signify concession of unpatentability of the claim prior to its amendment.

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Applicants ask that all claims be allowed. Please apply  
applicable charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

Date: \_\_\_\_\_

11/27/06



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